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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/046,671	Applicant(s) TAKITA ET AL.	
	Examiner Kurt M Eaton	Art Unit 2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

1)☒ Responsive to communication(s) filed on *17 September 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *8-22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☒ All b)☐ Some * c)☐ None of the CERTIFIED copies of the priority documents have been:

1.☒ received

2.☐ received in Application No. (Series Code / Serial Number) _____ .

3.☐ received in this National Stage application from the International Bureau (PCT Rule 17 2(a))

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

14) ☒ Notice of References Cited (PTO-892)
15) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
16) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
17) ☐ Interview Summary (PTO-413) Paper No(s) _____
18) ☐ Notice of Informal Patent Application (PTO-152)
19) ☐ Other:

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I, drawn to a semiconductor device (Claims 1-7) in Paper No. 4 is acknowledged.

2. Claims 8-22 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 4.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

6. Claims 1-3, 5, and 6 are rejected under 35 U.S.C. 102(a) as being anticipated by applicants admitted prior art.

In re claim 1, applicants admitted prior art shows a semiconductor device including:

a semiconductor substrate (114) of a first conduction type (p) {Figure 29A; page 4, lines 21-23};

a buried semiconductor layer of a second conduction type (n) formed in a first region (spanning regions 148 and 132 underneath structures depicted by reference numerals 164 and 138) of the semiconductor substrate, spaced from a surface of the semiconductor substrate {Figure 29A},

a semiconductor region (138) of the second conduction type extending from the surface of the semiconductor substrate to a peripheral portion of the buried semiconductor layer {Figure 29A; page 5, lines 19-23}; and

a semiconductor region (164) of the first conduction type formed in the semiconductor substrate surrounded by the buried semiconductor layer and the semiconductor region of the second conduction type {Figure 29A; page 6, lines 8-10}.

In re claim 2, applicants admitted prior art shows a semiconductor device according to claim 1, further including:

a first semiconductor element (146) formed in the first conduction type region {Figure 29A; page 6, lines 20-26}; and

a second semiconductor element (110) formed in a second region (112) different from the first region of the semiconductor substrate {Figure 29A; page 1, lines 23-26}, wherein

the first conduction type semiconductor region is connected to a first potential (V_{BL}) {Figure 29A}, and

the second region of the semiconductor substrate is connected to a second potential (V_{ss}) different from the first potential {Figure 29A}.

In re claim 3, applicants admitted prior art shows a semiconductor device according to claim 2, wherein:

the second conduction type semiconductor region is extended over a third region (132) adjacent to the first region of the semiconductor substrate {Figure 29A; page 5, lines 19-22};

the semiconductor device further includes a third semiconductor element (128) formed in the third region of the second conduction type semiconductor region {Figure 29A}; and

the second conduction type semiconductor region is connected to a third potential (V_{dd}) different at least from the first potential or the second potential {Figure 29A}.

In re claims 5 and 6, applicants admitted prior art shows a semiconductor device according to claims 2 and 3 wherein:

the first semiconductor element and/or the second semiconductor element is a memory cell {Figure 29A; page 3, lines 21-22}.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicants admitted prior art as applied to claims 1-3, 5, and 6 above.

Applicants admitted prior art substantially discloses the invention as claimed but fails to show a well of the first conduction type formed in a fourth region in the third region; and a fourth semiconductor element formed in the first conduction type well, wherein the first conduction type well is connected to a fourth potential different from at least the first potential.

It would have been obvious to one of ordinary skill in the art at the time the invention was made for the semiconductor device to have a well of the first conduction type formed in a fourth region in the third region and a fourth semiconductor element formed in the first conduction type well, wherein the first conduction type well is connected to a fourth potential different from at least the first potential since this would require mere duplication of structures parts from within the first region (i.e., duplication of the semiconductor region of the first conduction type formed in the semiconductor substrate surrounded by the buried semiconductor layer and the semiconductor region of the second conduction type which extends from the surface of the semiconductor substrate to a peripheral portion of the buried semiconductor layer; duplication of the first

semiconductor element formed in the first conduction type region; and duplication of the first conduction type semiconductor region being connected to the first potential) to within the third region adjacent to the first region of the semiconductor substrate and mere duplication of essential structures of a device involves only routine skill in the art.

Conclusion

9. Paper related to this application may be submitted directly to Art Unit 2823 by facsimile transmission. Papers should be faxed to Art Unit 2823 via the Art Unit 2823 Fax Center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2823 Fax Center number is **(703) 308-7722** or **–7724**. The Art Unit 2823 Fax Center is to be used only for papers related to Art Unit 2823 applications.

Any inquiry concerning this communication of earlier communication from the examiner should be directed to **Kurt Eaton** at **(703) 305-0383** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via kurt.eaton@uspto.gov.

WAEL FAHMY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800